Instruction Manual

Tektronix

TMS 141
8096, 80196 & 80C196 Microprocessor Support

070-9814-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 141 8096, 80196 and 80C196 microprocessor support and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor supports on the logic analyzer for which the TMS 141 8096, 80196 and 80C196 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor supports, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor supports is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names should be replaced with 8096. This is the name of the microprocessor in field selections and file names you must use to operate the 8096, 80196 and 80C196 support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 102/136-channel or a 96-channel module.
- 8096 refers to all supported variations of the 8096, 80196 and 80C196 microprocessor unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics:

- A description of the TMS 141 microprocessor support
- Logic analyzer software compatibility
- Your system under test requirements
- Support restrictions
- How to configure the probe adapter
- How to connect to the system under test (SUT)

Support Description

The TMS 141 microprocessor support disassembles data from systems that are based on the Intel 8096, 80196 and 80C196 microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 141 microprocessor support.

Table 1–1 shows the microprocessors and packages from which the TMS 141 support can acquire and disassemble data.

Table 1–1: Supported microprocessors

Name	Package
8096BH	68-pin PGA & PLCC
8397BH/JF	68-pin PGA & PLCC
8097BH/JF	68-pin PGA & PLCC
8797BH/JF	68-pin PGA & PLCC
8396BH/JF	68-pin PGA & PLCC
83C196KB	68-pin PGA & PLCC
80C196KB	68-pin PGA & PLCC
87C196KB	68-pin PGA & PLCC
87C196KB16	68-pin PLCC
87C196KC	68-pin PLCC

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *8096/196 Microprocessor User's Manual*, Intel, 1991.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the 8096, 80196 and 80C196 support, the Tektronix logic analyzer must be equipped with either a 102/136-channel module, or a 96-channel module at a minimum. The module must be equipped with enough probes to acquire clock and channel data from signals in your 8096, 80196 and 80C196-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other 8096, 80196 and 80C196 support requirements and restrictions.

System Clock Rate. The microprocessor support product supports the 8096 microprocessor at speeds of up to 12 MHz[1], the 80196 microprocessor at speeds of up to 16 MHz[1], and the 80C196 microprocessor at speeds of up to 16 MHz[1].

[1] **Specification at time of printing. Contact your logic analyzer sales representative for current information on the fastest devices supported.**

Configuring the Probe Adapter

To assure you acquire proper data for your SUT, you need to set jumpers on the probe adapter. Do this before connecting the probe adapter to the SUT.

Tables 1–2 and 1–3 show the jumper information for the PGA and PLCC probe adapters.

Table 1–2: PGA probe adapter jumpers

Name	Number	Jumper position	Configuration
CCR_2	J200	HI (1-2)	BHE~ & WR~
		LO (2-3)	WRH~ & WRL~
CCR_1	J160	HI (1-2)	Dynamic BUSWIDTH: 8 & 16 bit data bus
		LO (2-3)	Static BUSWIDTH: 8 bit data bus only
µP_Select	J300	8096 (1-2)	8096 Family
		80196 (2-3)	80196 Family

Table 1–3: PLCC probe adapter jumpers

Name	Number	Jumper position	Configuration
CCR_2	J1401	HI (1-2)	BHE~ & WR~
		LO (2-3)	WRH~ & WRL~
CCR_1	J1301	HI (1-2)	Dynamic BUSWIDTH: 8 & 16 bit data bus
		LO (2-3)	Static BUSWIDTH: 8 bit data bus only
µP_Select	J1701	8096 (1-2)	8096 Family
		80196 (2-3)	80196 Family

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. The probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

PGA Probe Adapter

To connect the logic analyzer to a SUT using a PGA probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–1. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the microprocessor from your SUT.
5. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–1.

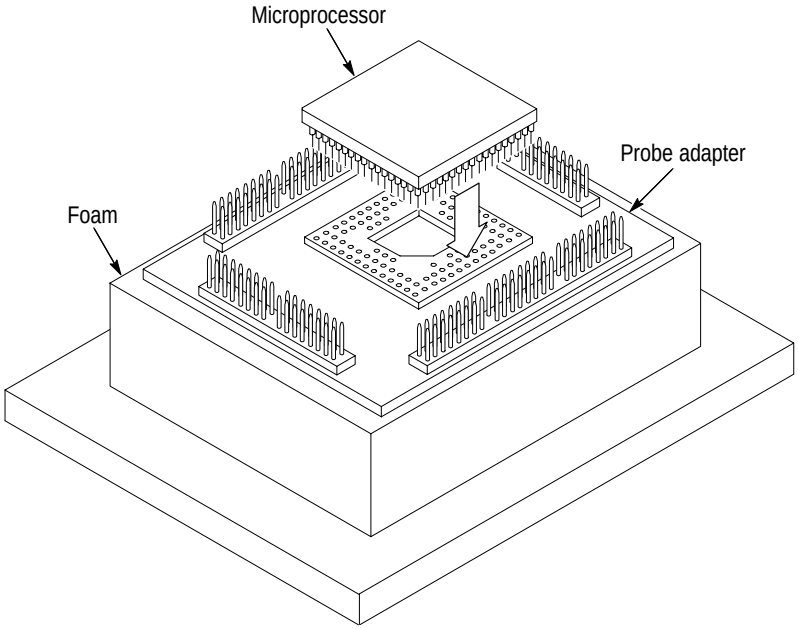


Figure 1–1: Placing a microprocessor into a PGA probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–2. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

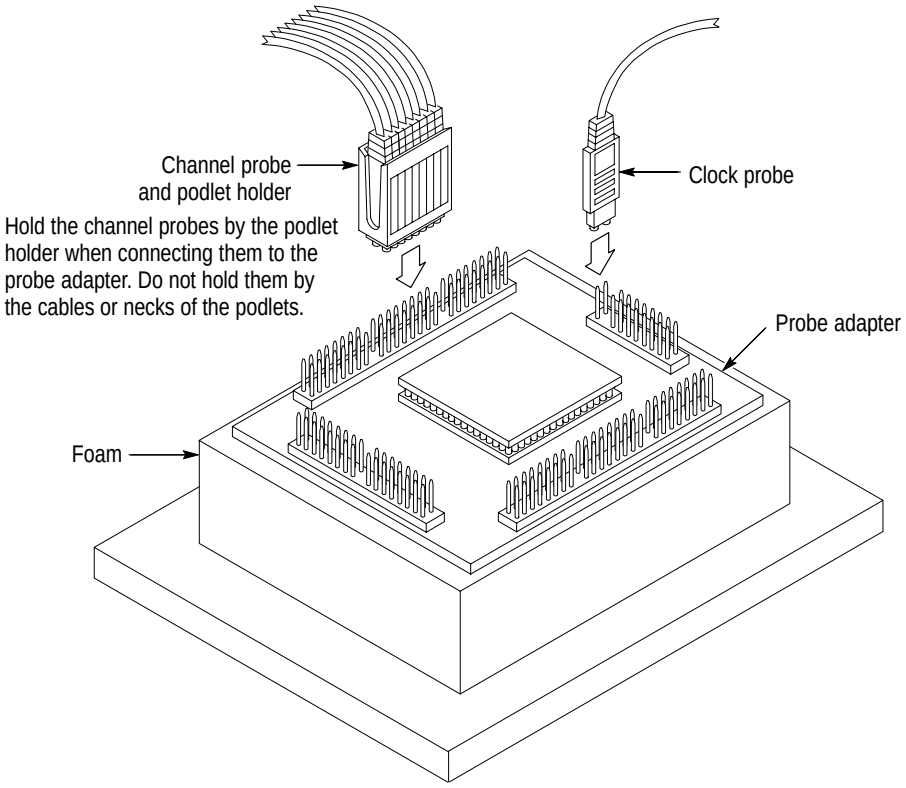


Figure 1–2: Connecting probes to a PGA probe adapter

8. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on your SUT.

9. Place the probe adapter onto the SUT as shown in Figure 1–3.

NOTE. *You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.*

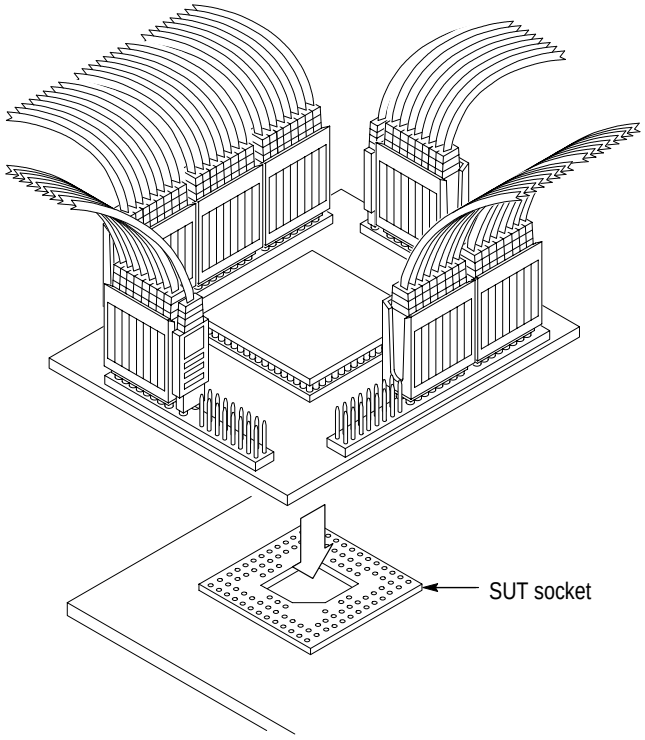


Figure 1–3: Placing a PGA probe adapter onto the SUT

PLCC Probe Adapter

To connect the logic analyzer to a SUT using a PLCC probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–4. This prevents the circuit board from flexing.
4. Remove the microprocessor from your SUT.

5. Line up the pin 1 indicator on the microprocessor with pin 1 of the PLCC socket on the probe adapter.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage all electrical components once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–4.

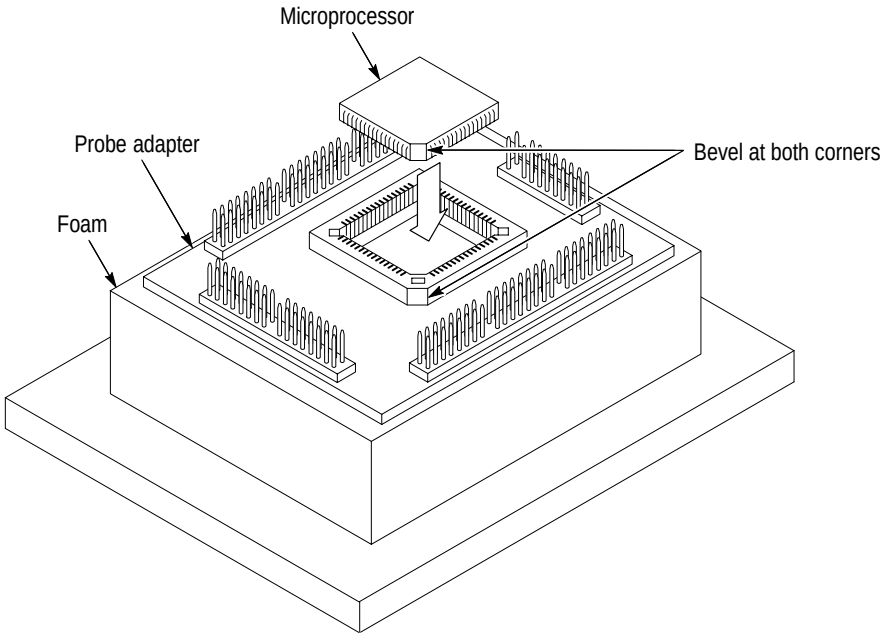


Figure 1–4: Placing a microprocessor into a PLCC probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–5. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

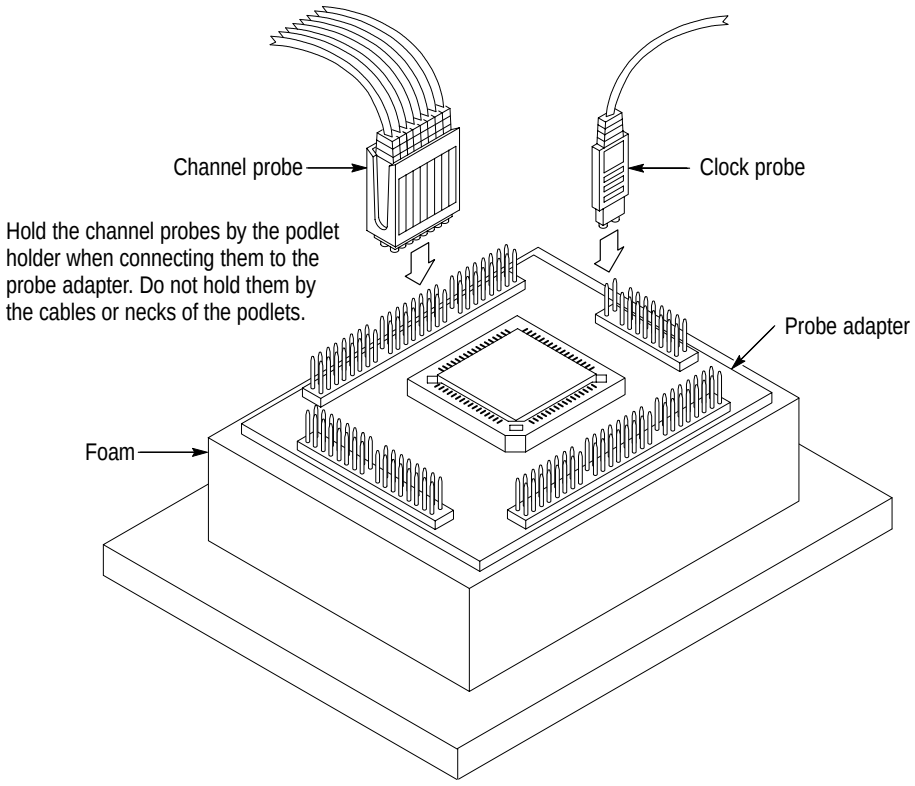


Figure 1–5: Connecting probes to a PLCC probe adapter

8. Place the probe adapter onto the SUT as shown in Figure 1–6.

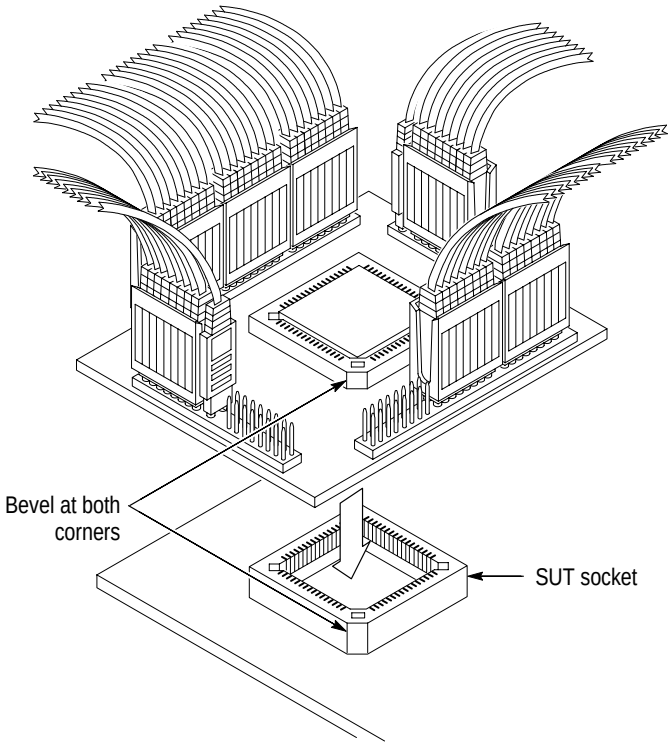


Figure 1–6: Placing a PLCC probe adapter onto the SUT

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to 8096, 80196 and 80C196 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

3. Use Table 1–4 to connect the channel probes to 8096, 80196 and 80C196 signal pins on the test clip or in the SUT.

Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Table 1–4: 8096, 80196 and 80C196 signal connections for channel probes

Section:channel	Signal name	Section:channel	Signal name
A2:7	WR~	A3:7	HSO.5/HSI.3
A2:6	BHE~	A3:6	HSO.4/HSI.2
A2:5	BUSWIDTH~	A3:5	HSI.1
A2:4	P2.3	A3:4	HSI.0
A2:3	P2.2	A3:3	HSO.3
A2:2	P2.1	A3:2	HSO.2
A2:1	P2.0	A3:1	HSO.1
A2:0	READY	A3:0	HSO.0
A1:7	A15	D1:7	D15
A1:6	A14	D1:6	D14
A1:5	A13	D1:5	D13
A1:4	A12	D1:4	D12
A1:3	A11	D1:3	D11
A1:2	A10	D1:2	D10
A1:1	A9	D1:1	D9
A1:0	A8	D1:0	D8
A0:7	A7	D0:7	D7
A0:6	A6	D0:6	D6
A0:5	A5	D0:5	D5
A0:4	A4	D0:4	D4
A0:3	A3	D0:3	D3
A0:2	A2	D0:2	D2
A0:1	A1	D0:1	D1
A0:0	A0	D0:0	D0
C2:7	ALE	C2:3	NMI
C2:6	RD~	C2:2	RESET~
C2:5	INST	C2:1	EA~
C2:4	CCR_2 †	C2:0	CLKOUT

† **Derived signal.**

Table 1–5 shows the clock probes and the 8096, 80196 and 80C196 signal to which they must connect for disassembly to be correct.

Table 1–5: 8096, 80196 and 80C196 signal connections for clock probes

Section:channel	8096, 80196 and 80C196 signal name	Section:channel	8096, 80196 and 80C196 signal name
CK:3	Not connected	CK:1	WR=~
CK:2	ALE=	CK:0	RD=~

= Indicates indicates the signal is double probed.

4. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the 8096, 80196 and 80C196 microprocessor in your SUT and attach the clip.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 141 8096, 80196 and 80C196 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the 8096, 80196 and 80C196 support are Address, Data, Control, Misc, HSI_0, and Port_2. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–6.

Clocking Options

The TMS 141 support offers a microprocessor-specific clocking mode for the 8096, 80196 and 80C196 microprocessor. This clocking mode is the default selection whenever you load the 8096 support.

No clocking options are available.

A description of how cycles are sampled by the module using the TMS 141 support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

Symbols

The TMS 141 support supplies one symbol table file. The 8096_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file 8096_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value CCR_2 ALE_B BUSWTH_L NST BHE_BB~ WR_BB~ RD_B~	Meaning
FETCH_BYT	X 0 0 1 X 1 0	Instruction Fetch Byte
FETCH_WD	X 0 1 1 X 1 0	Instruction Fetch Word
FETCH *	X 0 X 1 X 1 0	Instruction Fetch
READ_BYT	X 0 0 0 X 1 0	Byte Read
READ_WD	X 0 1 0 X 1 0	Word Read
READ *	X 0 X 0 X 1 0	Read Cycle
WRITE_BYT	X 0 0 0 X X 1	Byte Write
WRITE_WD	X 0 1 0 X X 1	Word Write
WRITE *	X 0 X 0 X X 1	Write Cycle

***** **Use only for triggering**

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- How to change the way data is displayed
- How to change disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 8096 support, choose a clocking mode and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual, whichever is available.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–6.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows these special characters and strings, and gives a definition of what they represent.

Table 2–2: Meaning of special characters in the display

Character or string displayed	Meaning
≫ or m	The instruction was manually marked as a program fetch
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks will indicate the width of the data that is unavailable. Each two asterisks represent a byte.

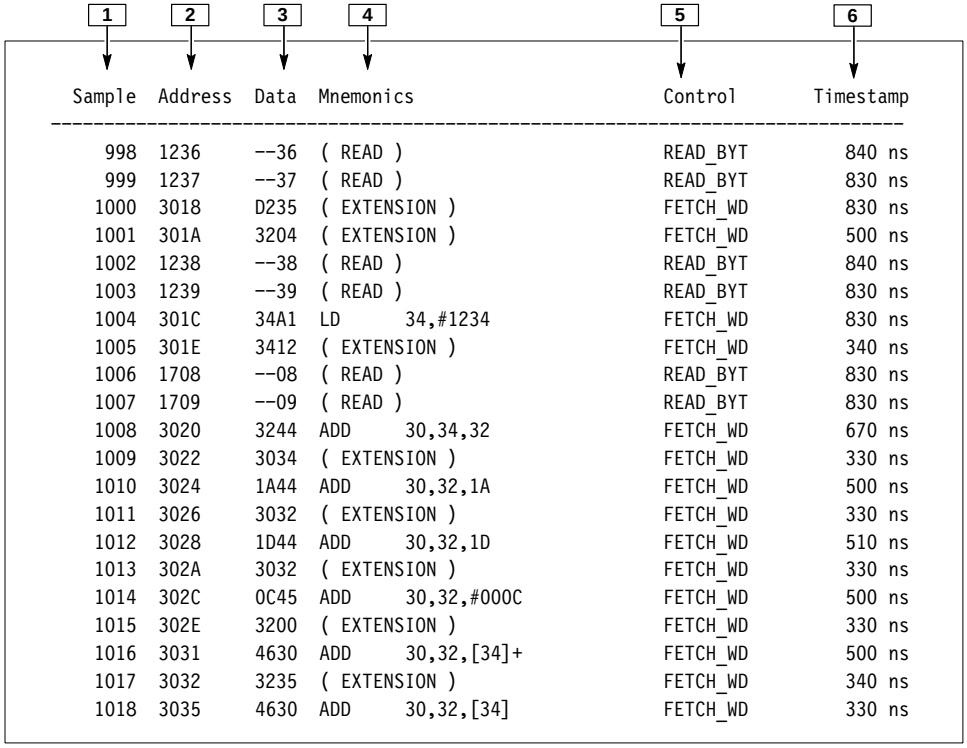
Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–3: Cycle type definitions

Cycle type	Definition
UNKNOWN	Unknown cycle type
FLUSH	Fetch cycle computed to be flushed
READ	Read cycle
WRITE	Write cycle
EXTENSION	Fetch cycle computed to be an opcode extension
REFETCH	Fetch cycle computed to be an opcode refetch
RESET	Resets the microprocessor to a known state
TIMER OVERFLOW VECTOR	Timer Vector
A/D CONVERSON VECTOR	A/D Vector
HSI DATA VECTOR	HSI Vector
HIGH SPEED O/P VECTOR	HSO Vector
HSI. O VECTOR	HSI. O Vector
S/W TIMERS VECTOR	S/W Timer Vector
SERIAL PORT VECTOR	Serial Port Vector
EXT INT/NMI VECTOR	External Interrupt Vector
TRAP VECTOR	TRAP Vector

Figure 2–1 shows an example of the Hardware display.



Sample	Address	Data	Mnemonics	Control	Timestamp
998	1236	--36	(READ)	READ_BYT	840 ns
999	1237	--37	(READ)	READ_BYT	830 ns
1000	3018	D235	(EXTENSION)	FETCH_WD	830 ns
1001	301A	3204	(EXTENSION)	FETCH_WD	500 ns
1002	1238	--38	(READ)	READ_BYT	840 ns
1003	1239	--39	(READ)	READ_BYT	830 ns
1004	301C	34A1	LD 34,#1234	FETCH_WD	830 ns
1005	301E	3412	(EXTENSION)	FETCH_WD	340 ns
1006	1708	--08	(READ)	READ_BYT	830 ns
1007	1709	--09	(READ)	READ_BYT	830 ns
1008	3020	3244	ADD 30,34,32	FETCH_WD	670 ns
1009	3022	3034	(EXTENSION)	FETCH_WD	330 ns
1010	3024	1A44	ADD 30,32,1A	FETCH_WD	500 ns
1011	3026	3032	(EXTENSION)	FETCH_WD	330 ns
1012	3028	1D44	ADD 30,32,1D	FETCH_WD	510 ns
1013	302A	3032	(EXTENSION)	FETCH_WD	330 ns
1014	302C	0C45	ADD 30,32,#000C	FETCH_WD	500 ns
1015	302E	3200	(EXTENSION)	FETCH_WD	330 ns
1016	3031	4630	ADD 30,32,[34]+	FETCH_WD	500 ns
1017	3032	3235	(EXTENSION)	FETCH_WD	340 ns
1018	3035	4630	ADD 30,32,[34]	FETCH_WD	330 ns

Figure 2–1: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the 8096, 80196 and 80C196 Address bus.

3 **Data Group.** Lists data from channels connected to the 8096, 80196 and 80C196 Data bus.

4 **Mnemonics Column.** Lists the disassembled instructions and cycle types.

5 **Control Group.** Lists data from channels connected to microprocessor control signals (shown symbolically).

6 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. The display is designed to resemble assembly language listings.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the 8096, 80196 and 80C196 microprocessor are as follows:

SJMP	JBC	JNC	JST	JV	BR
LJMP	JBS	JNVT	JH	JLT	TRAP
SCALL	JNST	JNV	JLE	JE	RST
LCALL	JNH	JGE	JC	DJNZ	
RET	JGT	JNE	JVT	DJNZW (80196 only)	

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the 8096, 80196 and 80C196 microprocessor are as follows:

SCALL	LCALL	RET	TRAP	RST

Changing How Data is Displayed

There are fields and features that allow you to further modify displayed data to suit your needs. You can make selections unique to the 8096, 80196 and 80C196 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles

Optional Display Selections

You can make optional display selections for disassembled data to help you analyze the data. You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

In addition to the common display options (described in the information on basic operations), you can select the microprocessor from which to acquire and disassemble data.

You can use the InstrSet field to select the microprocessor that you are testing, either 8096 or 80196. You must also set the jumper on the probe adapter board (J300 on the PGA probe adapter or J1750 on the PLCC probe adapter) for the microprocessor you want. If you do not select the correct microprocessor, your disassembled data might be incorrect.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)
- Anything (any valid opcode, extension or flush)

Mark selections for a 16-bit bus are as follows:

```
Any          Opcode
Opcode       Extension
Opcode       Flush
Flush        Extension
Flush        Flush

Undo Mark
```

Mark selections for an 8-bit bus are as follows:

```
OPCODE
Ext
Flush

Undo Mark
```

Information on basic operations contains more details on marking cycles.

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your 8096, 80196 and 80C196 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires 8096, 80196 and 80C196 signals
- List of other accessible microprocessor signals and extra acquisition channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a 8096, 80196 and 80C196 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

The two probe adapters accommodate the Intel 8096, 80196 and 80C196 microprocessor in 68-pin PGA and 68-pin PLCC packages.

Configuration

The probe adapter contains jumpers that need to be in certain positions for proper disassembly; Tables 3–1 and 3–2 show the jumper positions.

Table 3–1: PGA probe adapter jumpers

Name	Number	Jumper position	Configuration
CCR_2	J200	HI (1-2)	BHE~ & WR~
		LO (2-3)	WRH~ & WRL~
CCR_1	J160	HI (1-2)	Dynamic BUSWIDTH: 8 & 16 bit data bus
		LO (2-3)	Static BUSWIDTH: 8 bit data bus only
µP_Select	J300	8096 (1-2)	8096 Family
		80196 (2-3)	80196 Family

Table 3–2: PLCC probe adapter jumpers

Name	Number	Jumper position	Configuration
CCR_2	J1401	HI (1-2)	BHE~ & WR~
		LO (2-3)	WRH~ & WRL~
CCR_1	J1301	HI (1-2)	Dynamic BUSWIDTH: 8 & 16 bit data bus
		LO (2-3)	Static BUSWIDTH: 8 bit data bus only
µP_Select	J1701	8096 (1-2)	8096 Family
		80196 (2-3)	80196 Family

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–3 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–3, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–3: Electrical specifications

Characteristics	Requirements
SUT DC power requirements	
Voltage	4.75-5.25 VDC
Current	< 250 mA
SUT clock	
Clock rate	
8096BH	6 to 12 MHz
80196KB	3.5 to 16 MHz
80196KC	8 to 16 MHz
Minimum setup time required	
Address w/respect to falling edge of ALE/ADV~	5.0 ns
Data w/respect to rising edge of RD~	3.5 ns
Data w/respect to rising edge of WR~/WRL~	5.0 ns
Data w/respect to BHE~/WRH~	5.0 ns
BUSWTH (8096) w/respect to falling edge of ALE/ADV~ and rising edge of CLKOUT	10 ns
BUSWTH (80196) w/respect to falling edge of ALE/ADV~ and falling edge of CLKOUT	10 ns
All Other Signals	5 ns
Minimum hold time required	
Address w/respect to falling edge of ALE/ADV~	0 ns
Data w/respect to rising edge of RD~	4.8 ns
Data w/respect to rising edge of WR~/WRL~	4.8 ns
Data w/respect to BHE~/WRH~	0 ns
BUSWTH (8096) w/respect to falling edge of ALE/ADV~ and rising edge of CLKOUT	4 ns
BUSWTH (80196) w/respect to falling edge of ALE/ADV~ and falling edge of CLKOUT	4 ns
All Other Signals	0 ns
Timing Violations	
Data w/respect to rising edge of RD~	Th (min) = 4.8 ns
BUSWTH (8096) w/respect to falling edge of ALE/ADV~ and rising edge of CLKOUT	Th (min) = 4 ns
BUSWTH (80196) w/respect to falling edge of ALE/ADV~ and falling edge of CLKOUT	Th (min) = 4 ns

Table 3–3: Electrical specifications (cont.)

Characteristics	Requirements	
	Specification	
Measured typical SUT signal loading	AC load	DC load
AD0-AD15	5 pF + podlet	podlet
HSI.0-HSI.3	5 pF + podlet	podlet
HS0.0-HS0.3	5 pF + podlet	podlet
P2.0-P2.3, INST, EA~, READY, RESET~, NMI	10 pF + podlet	podlet
BHE~, WR~	16 pF	one 74FCT541A in parallel w/one 20L8-5
CLKOUT	10 pF	one 74FCT541A in parallel w/one 20L8-5
ALE, RD~, BUSWTH	10 pF	one 74FCT541A

Table 3–4 shows the environmental specifications.

Table 3–4: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed 8096, 80196 and 80C196 microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–5 shows the certifications and compliances that apply to the probe adapter.

Table 3–5: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.

Figure 3–1 shows the PGA probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

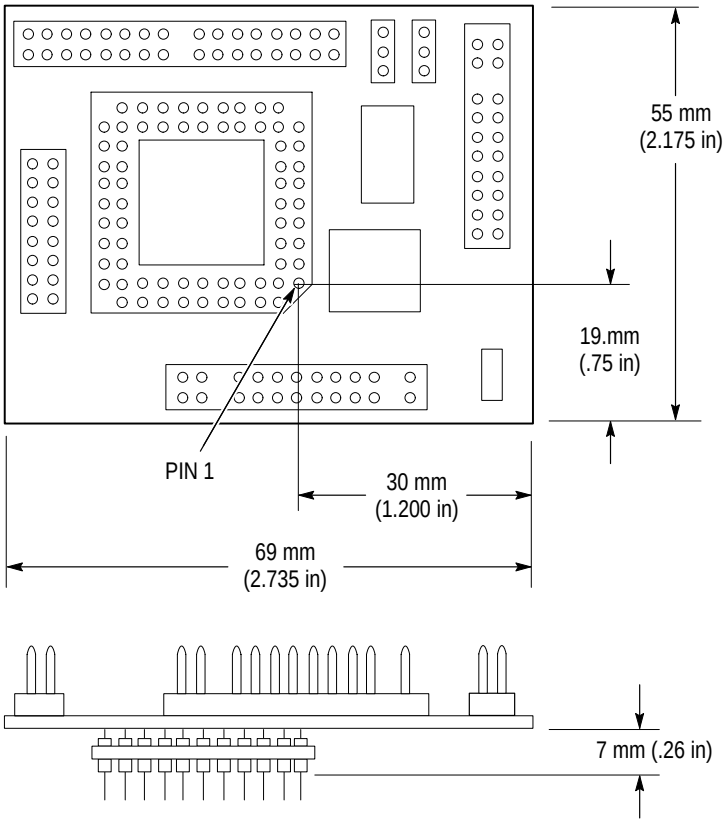


Figure 3–1: Minimum clearance of the PGA probe adapter

Figure 3–2 shows the PLCC probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

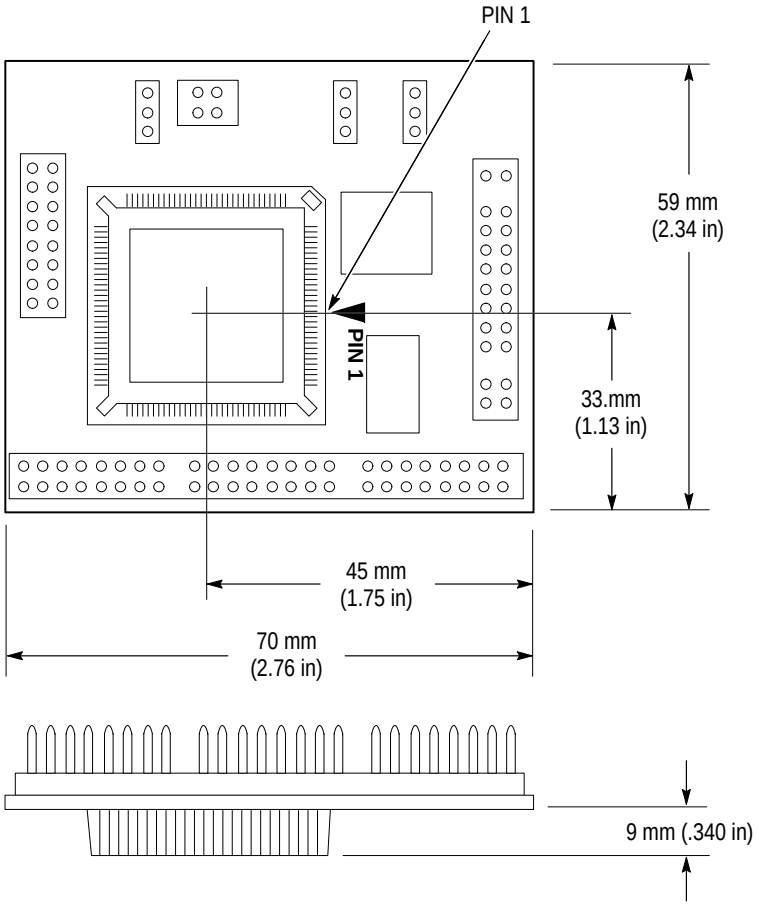


Figure 3–2: Minimum clearance of the PLCC probe adapter

Channel Assignments

Channel assignments shown in Table 3–6 through Table 3–12 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.
- An _L indicates that the signal is latched.
- An _B indicates that the signal is buffered.
- An _BB indicates that the signal is double buffered.

Table 3–6 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–6: Address group channel assignments

Bit order	Section:channel	8096, 80196 and 80C196 signal name
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 3–7 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–7: Data group channel assignments

Bit order	Section:channel	8096, 80196 and 80C196 signal name
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8

Table 3–7: Data group channel assignments (cont.)

Bit order	Section:channel	8096, 80196 and 80C196 signal name
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–8 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–8: Control group channel assignments

Bit order	Section:channel	8096, 80196 and 80C196 signal name	Derived signal name
6	C2:4		CCR_2
5	C2:7	ALE	ALE_B
4	A2:5	BUSWIDTH~	BUSWTH_L
3	C2:5	INST	INST
2	A2:6	BHE~	BHE_BB~
1	A2:7	WR~	WR_BB~
0	C2:6	RD~	RD_B~

Table 3–9 shows the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–9: Misc group channel assignments

Bit order	Section:channel	8096, 80196 and 80C196 signal name	Derived signal name
4	C2:0	CLKOUT	CLKOUT_B
3	C2:3	NMI	NMI

Table 3–9: Misc group channel assignments (cont.)

Bit order	Section:channel	8096, 80196 and 80C196 signal name	Derived signal name
2	C2:1	EA~	EA~
1	A2:0	READY	READY
0	C2:2	RESET~	RESET~

Table 3–10 shows the section and channel assignments for the Port_2 group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–10: Port_2 group channel sssignments

Bit order	Section:channel	8096, 80196 and 80C196 signal name	Derived signal name
3	A2:4	P2.3	P2_3
2	A2:3	P2.2	P2_2
1	A2:2	P2.1	P2_1
0	A2:1	P2.0	P2_0

Table 3–11 shows the section and channel assignments for the HSI_O group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–11: HSI_O group channel sssignments

Bit order	Section:channel	8096, 80196 and 80C196 signal name	Derived signal name
7	A3:7	HSO.5/HSI.3	HSI_3
6	A3:6	HSO.4/HSI.2	HSI_2
5	A3:5	HSI.1	HSI_1
4	A3:4	HSI.0	HSI_0
3	A3:3	HSO.3	HSO_3
2	A3:2	HSO.2	HSO_2
1	A3:1	HSO.1	HSO_1
0	A3:0	HSO.0	HSO_0

Table 3–12 shows the section and channel assignments for the clock channels (not part of any group) and the microprocessor signal to which each channel connects.

Table 3–12: Clock channel sssignments

Bit order	Section:channel	8096, 80196 and 80C196 signal name	Derived signal name
CK:2	Falling	ALE	ALE_B=
CK:1	Rising	WR~	WR_D~
CK:0	Rising	RD~	RD_B~=

How Data is Acquired

This part of this chapter explains how the module acquires 8096, 80196 and 80C196 signals using the TMS 141 software and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

A special clocking program is loaded to the module every time you load the 8096 support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the 8096, 80196 and 80C196 bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–3 shows the sample points and the master sample point for the 8096 bus timing. Figure 3–4 shows the sample points and the master sample point for the 80196 and 80C196 bus timing.

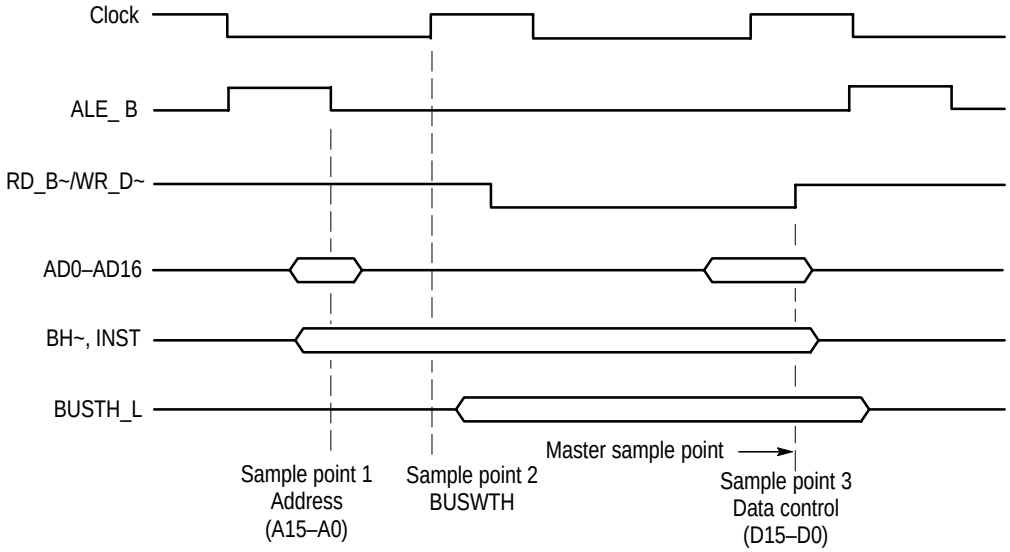


Figure 3–3: 8096 bus timing

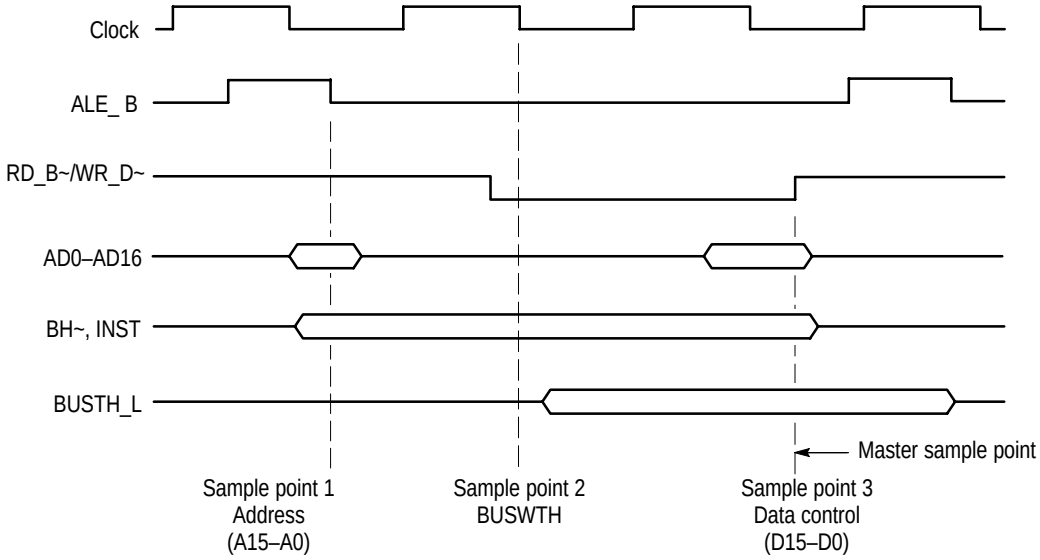


Figure 3–4: 80196 and 80C196 bus timing

There are no clocking options.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so that you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–6. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals Not On the Probe Adapter

The probe adapter does not provide access for the following microprocessor signals:

- P2.4 – P2.7
- P1.0 – P1.7
- P0.0 – P0.7
- XTAL1
- XTAL2

Extra Channels

Table 3–13 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Table 3–13: Extra module sections and channels

Module	Section: channels
102-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0
136-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0, E3:7-0, E2:7-0, E1:7-0, E0:7-0
96-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0

Extra channels are logged in with the Master Sample Point.

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This chapter contains the circuit description for the probe adapters.

Probe Adapter Circuit Description

The probe adapters use the 74FCT541A to reduce the DC and AC loading that is placed upon the microprocessor's critical control lines. The 74F5074 latches the BUSWTH from the SUT. A PAL, 20L8-5, tracks ALE and CLKOUT to determine when BUSWTH is valid. When valid, the PAL 20L8-5 will clock BUSWTH into the register. On the 8096, BUSWTH is sampled on the first rising edge of CLKOUT after ALE falls. On the 80196 and 80C196, BUSWTH is sampled on the first falling edge of CLKOUT after ALE falls.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 141 8096, 80196 and 80C196 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

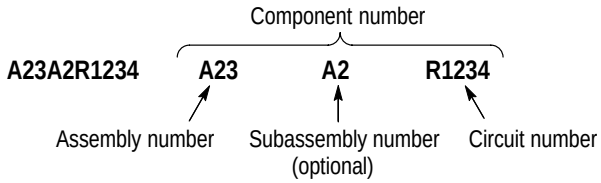
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK0875	MATSUO ELECTRONICS INC	831 S DOUBLAS ST	EL SEGUNDO CA 92641
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
1CH66	PHILIPS SEMICONDUCTORS	811 E ARQUES AVENUE PO BOX 3409	SUNNYVALE CA 94088–3409
61772	INTEGRATED DEVICE TECHNOLOGY	3236 SCOTT BLVD	SANTA CLARA CA 95051
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	671–2558–00			CIRCUIT BD ASSY:8096/196 SPT,PROBE ADAPTER, PGA68,SOCKETED;	80009	671255800
A02	671–2559–00			CIRCUIT BD ASSY:8096/196 SPT,PROBE ADAPTER, PLCC68,SOCKETED;	80009	671255900
A01	671–2558–00			CIRCUIT BD ASSY:8096/196 SPT,PROBE ADAPTER, PGA68,SOCKETED;	80009	671255800
A01C170	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A01C220	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A01C260	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A01C640	290–5005–00			CAP,FXD,TANT:47MF,10%,10V,SMD,T&R	TK0875	267M–1002–476–K
A01C740	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A01J150	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIGURE 1)	80009	131526700
A01J160	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION (SEE RMPL FIGURE 1)	00779	104344–1
A01J200	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION (SEE RMPL FIGURE 1)	00779	104344–1
A01J300	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION (SEE RMPL FIGURE 1)	00779	104344–1
A01J600	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIGURE 1)	80009	131526700
A01J790	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIGURE 1)	80009	131526700
A01J940	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIGURE 1)	80009	131526700
A01P160	—— ——			CONN,BOX:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER (SEE RMPL FIGURE 1)		
A01P200	—— ——			CONN,BOX:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER (SEE RMPL FIGURE 1)		
A01P300	—— ——			CONN,BOX:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER (SEE RMPL FIGURE 1)		
A01U180	156–5908–00			IC,DIGITAL:FTTL,FLIP FLOP;DUAL D–TYPE, METASTABLE IMMUNITY	1CH66	N74F5074D
A01U330	156–5793–00			IC,DIGITAL:FCTCMOS,BUFFER;OCTAL, 3–STATE		
A01U360	160–8991–00			IC,DIGITAL:STTL,PLD;PAL,20L8,5NS,210MA,PRGM	80009	160–8991–00
A01U460	—— ——			SOCKET,PGA:PCB,;68 POS,11 X 11,0.1 CTR X 0.1 CTR 0.17 H X 0.273 TAIL,OPEN CTR, SYMMETRICAL (SEE RMPL FIGURE 1)		

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A02	671–2559–00			CIRCUIT BD ASSY:8096/196 SPT,PROBE ADAPTER, PLCC68,SOCKETED;	80009	671255900
A02C1101	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A02C1251	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A02C1321	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A02C1511	290–5005–00			CAP,FXD,TANT:47MF,10%,10V,SMD,T&R	TK0875	267M–1002–476–K
A02C1961	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A02J1181	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIGURE 2)	80009	131526700
A02J1301	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION (SEE RMPL FIGURE 2)		
A02J1401	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION (SEE RMPL FIGURE 2)		
A02J1601	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIGURE 2)	80009	131526700
A02J1701	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION (SEE RMPL FIGURE 2)	80009	131526700
A02J1921	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIGURE 2)	80009	131526700
A02J1991	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	80009	131526700
A02P1301	—— ——			CONN,BOX:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER (SEE RMPL FIGURE 2)	26742	9618–302–50
A02P1401	—— ——			CONN,BOX:SHUNT/SHORTING,;FEMALE,1 X 2,0.1CTR,0.630 H,BLK,W/HANDLE,JUMPER (SEE RMPL FIGURE 2)		
A02P1701	—— ——			CONN,BOX:SHUNT/SHORTING,;FEMALE,1 X 2,0.1CTR,0.630 H,BLK,W/HANDLE,JUMPER (SEE RMPL FIGURE 2)		
A02P2641	—— ——			CONN,ADPT:SMD,PLCC;MALE,STR,68 POS,0.05 CTR,0.268H, PLCC MALE TOSMD PADS (NOT REPLACEBLE ORDER 671–2559–00)		
A02U1111	156–5908–00			IC,DIGITAL:FTTL,FLIP FLOP;DUAL D–TYPE, META STABLE IMMUNITY	1CH66	N74F5074D
A02U1341	160–8991–00			IC,DIGITAL:STTL,PLD;PAL,20L8,5NS,210MA,PRGM	80009	160–8991–00
A02U1371	156–5793–00			IC,DIGITAL:FCTCMOS,BUFFER;OCTAL, 3–STATE	61772	IDT74FCT541ASO
A02U1651	—— ——			SOCKET,PLCC SMD,;68 POS,0.05 CTR (NOT REPLACEABLE ORDER 671–2559–XX)		

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 141 8096, 80196 and 80C196 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656–4548
63058	MCKENZIE TECHNOLOGY	44370 OLD WARMS SPRINGS BLVD	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0545–00			1	PROBE ADAPTER:8096/196 SPT,PGA68, SOCKETED,(LASI III)	80009	010054500
–1	——— ———			2	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (SEE REPL A01 J150,J600,J790,J940)	80009	131526700
–2	131–4356–00			3	CONN,BOX:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER (P160,P200,P300)	26742	9618–302–50
–3	——— ———			2	CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION (SEE REPL A01 J160,J200,J300)		
–4	671–2558–00			1	CIRCUIT BD ASSY:8096/196 SPT,PROBE ADAPTER, PGA68,SOCKETED	80009	671255800
–5	136–0922–00			2	SOCKET,PGA:PCB,;68 POS,11 X 11,0.1 CTR X 0. 1 CTR 0.17 H X 0.273 TAIL,OPEN CTR (U460)	63058	PGA 68H115B1–11
					STANDARD ACCESSORIES		
	070–9814–00			1	MANUAL,TECH:INSTRUCTION,8096,DISSASEMBLER, TMS 141	80009	070–9814–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORY		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00

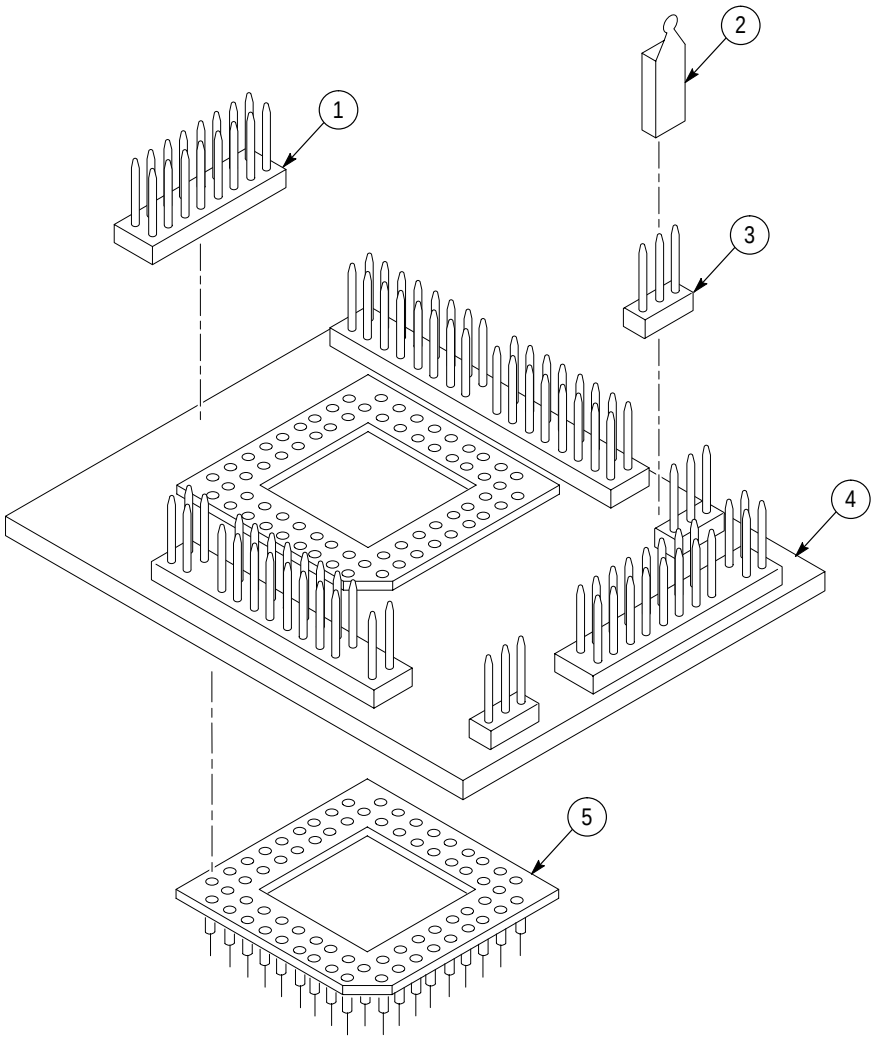


Figure 1: 8096, 80196 and 80C196 PGA probe adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
2–1	—— ——			1	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (SEE A02 REPL J1181,J1601,J1921,J1991)		
–2	131–4356–00			3	CONN,BOX:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 C TR,0.630 H,BLK,W/HANDLE,JUMPER (P1301,P1701,P1401)	26742	9618–302–50
–3	—— ——			3	CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION (SEE A02 REPL J1301,J1701,J1401)		
–4	671–2559–00			1	CIRCUIT BD ASSY:8096/196 SPT,PROBE ADAPTER, PLCC68,SOCKETED;	80009	671255900
					STANDARD ACCESSORIES		
	070–9814–00			1	MANUAL,TECH:INSTRUCTION,8096,DISSASEMBLER, TMS 141	80009	070–9814–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORY		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00

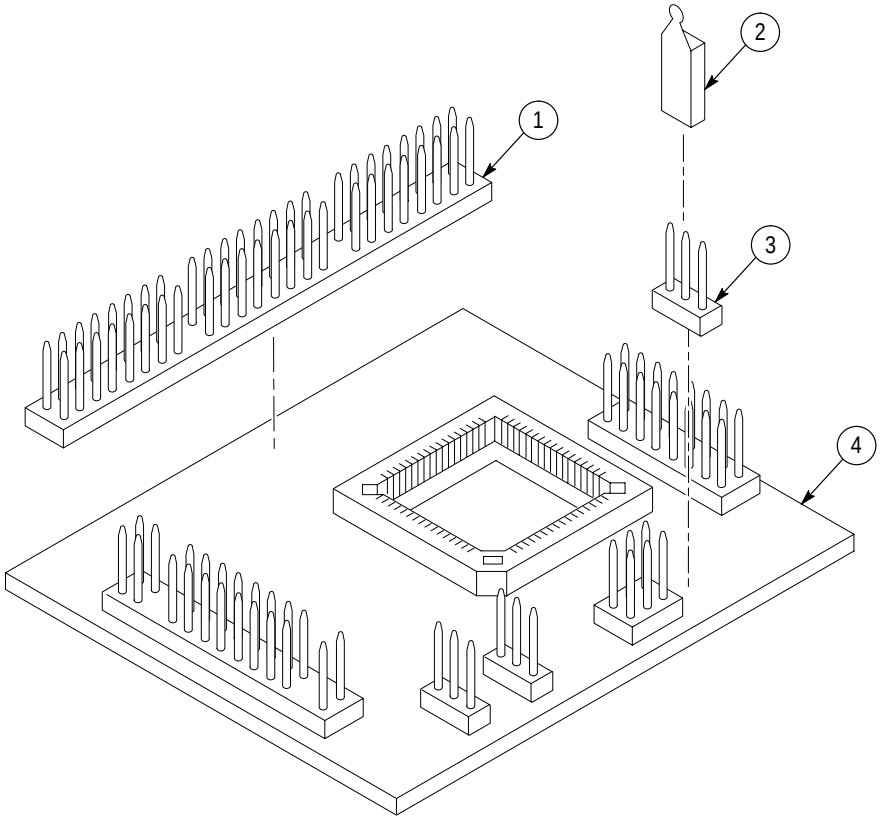


Figure 2: 8096, 80196 and 80C196 PLCC probe adapter exploded view

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